

CASCODED POWER AMPLIFIER, PARTICULARLY
FOR USE IN RADIO FREQUENCY

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present disclosure generally relates to a cascoded power amplifier, particularly but not exclusively for use in radio frequency applications. More specifically but not exclusively, the disclosure relates to a power amplifier comprising at least a load element and at least an active element inserted, in series to each other, between a first and a second voltage reference.

10 The disclosure relates particularly, but not exclusively, to a power amplifier for radio frequency applications and the following description is made with reference to this field of application for convenience of illustration only.

Description of the Related Art

As it is well known, radio frequency power amplifiers, or RF amplifiers, require high cut off frequencies as well as high breakdown voltage values in order to be able to provide high powers at high frequencies. Moreover, low feedback capacitance values, high transconductance values and low on-state resistance values are required.

20 Generally, some of these features are available in the VLSI CMOS BiCMOS and BCD standard silicon technologies. However, devices produced according to these technologies having all the above features simultaneously do not exist.

25 In particular, LDMOS devices ensure high breakdown voltage values as well as high power values, but they have degraded radio frequency performances.

On the contrary, VLSI CMOS devices, particularly transistors with short gate length, have a high transconductance, high frequency response and low on-state resistance, but a low breakdown voltage value.

BRIEF SUMMARY OF THE INVENTION

5 One embodiment of the invention uses a DMOS transistor and a CMOS transistor being conveniently connected in cascode configuration so as to obtain a power amplifier having optimum characteristics in radio frequency applications.

10 The features and advantages of the power amplifier according to the invention will be apparent from the following description of an embodiment thereof given by way of non-limiting example with reference to the attached drawing.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1 shows a power amplifier according to an embodiment of the invention.

15 DETAILED DESCRIPTION OF THE INVENTION

Embodiments of a cascoded power amplifier, particularly for use in radio frequency, are described herein. In the following description, numerous specific details are given to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the 20 invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to "one embodiment" or "an 25 embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the

present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in 5 one or more embodiments.

The technical problem underlying an embodiment of the present invention is to provide a power amplifier, having such structural and functional characteristics so as to allow high cut off frequencies, high breakdown voltage value, high transconductance values and low on-state resistance values to be 10 obtained, thus overcoming the limits still affecting at present the devices according to the prior art and allowing a right use thereof for radio frequency applications.

With reference to the sole drawing of Figure 1, a power amplifier according to one embodiment of the invention is globally and schematically indicated with 1.

15 The power amplifier 1 comprises a load element 2 and an active element 3, inserted in series to each other between a first voltage reference, in particular the supply voltage Vdd, and a second voltage reference, in particular the ground GND.

The load element 2 and the active element 3 are connected to each 20 other to define a circuit node X which can also serve as an additional output terminal of the power amplifier 1. The main output terminal is node Vdd.

In the example shown in the figure, the load element 2 comprises a DMOS transistor M1 having a gate terminal G1 receiving a first control voltage Vg1.

25 On the contrary, the active element 3 comprises a VLSI CMOS transistor M2 having a gate terminal G2 receiving a second control voltage Vg2. A high frequency bipolar transistor could also be used.

Advantageously, according to an embodiment of the invention, once the integration limits of the transistor M2 are fixed, the transistor M1 is sized and

biased in order to optimize the cascode configuration performances of the power amplifier 1, the power consumption and the reliability.

In particular, a value of the second control voltage V_{g2} is set and the integration limits of the transistor M1 are fixed in order to allow the transistor M2 to work in saturation area. In this way, the power amplifier 1 has in fact a high cut off frequency as well as a high transconductance value. In the linear area, a low activation resistance value is obtained.

It is worth noting that, advantageously, according to an embodiment of the invention, the transistor M2, working in saturation area, limits the peak voltage value in correspondence with the circuit node X to the gate-drain value that said transistor M2 can afford, *i.e.*:

$$V_x \geq (V_{g2} - V_{th2})$$

being:

15 V_x the voltage on the circuit node X;
 V_{g2} the voltage applied to the gate terminal G2 of the transistor M2; and

V_{th2} the threshold voltage of the transistor M2.

20 In an alternative embodiment, a resistive element is connected between the drain and source terminals of the transistor M2 so as to ensure the right stabilization of the circuit node X.

Direct current and alternating current simulations performed by the Applicant between an amplifier realized according to an embodiment of the invention by means of a DMOS transistor and a cascode configuration VLSI CMOS transistor and an amplifier realized according to the prior art by means of a 25 LDMOS transistor alone have shown the following performance improvements (to be considered only as indicative):

cut off frequency increase by more than 185%;

decrease by 50% in the product of the activation resistance and the CMOS channel length ($R_{on} \cdot W$);

early voltage (V_{early}) huge increase by about 30 times;

transconductance ($gm \cdot W$) increase by 150%;

5 feedback capacitance value (C_{gd}) decrease by 95%;

breakdown voltage increase. The power amplifier 1 failure is generally equal or higher than the transistor M1 (load) failure and it is certainly higher than the transistor M2 (active element) failure.

Moreover it must be noticed that the cascode configuration power 10 amplifier 1 according to one embodiment of the invention provides an area occupation depending on the sizing methodology applied. For example, the optimization of the knee current cascode amplifier can provide an area consumption corresponding to about 2-2.5 times an amplifier realized by means of a single DMOS transistor, with a corresponding increase in the output capacity 15 being almost doubled.

In conclusion, the cascaded power amplifier according to one embodiment of the invention has high cut off frequencies, high breakdown voltage values and high transconductance values in saturated area and low on-state resistance value, being therefore particularly suitable for radio frequency 20 applications.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

25 The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes,

various equivalent modifications are possible within the scope of the invention and can be made without deviating from the spirit and scope of the invention.

These and other modifications can be made to the invention in light of the above detailed description. The terms used in the following claims should

- 5 not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.